

partition region **2** in the active section **K** is $2.0 \times 10^{15} \text{ cm}^{-3}$. The width of p-type semiconductor region **22** in the edge termination section **S** is 8.5 μm , 8.3 μm , 8.1 μm , and 7.9 μm from the active section **K** side to the edge of the edge termination section **S**. The impurity concentration in p-type semiconductor region **22** and in n-type semiconductor region **21** in the edge termination section **S** is $2.0 \times 10^{15} \text{ cm}^{-3}$. The diffusion depth of p-type guard ring regions **32a**, **32b**, and **32c** is 3.0 μm . The surface impurity concentration in p-type guard ring regions **32a**, **32b**, and **32c** is $3.0 \times 10^{17} \text{ cm}^{-3}$.

[0047] According to the first embodiment, the robustness against induced charges for the breakdown voltage is maintained by setting the width of p-type semiconductor region **22** in the edge termination section **S** to be narrower from the active section **K** toward the edge of the edge termination section **S**. The p-type impurity amount becomes smaller gradually by setting p-type semiconductor region **22** to be narrower from the active section **K** toward the edge of the edge termination section **S** and the n-type impurity amount becomes larger gradually by setting n-type semiconductor region **21** to be wider from the active section **K** toward the edge of the edge termination section **S** to maintain the robustness against induced charges for the breakdown voltage.

[0048] The widths of p- and n-type semiconductor region **22** and **21** are set as described above due to the reason described below. The structure described above makes it easier for a depletion layer to expand on the active section side due to positive charges and harder for the depletion layer to expand on the edge side of the edge termination section **S** due to negative charges.

[0049] In FIG. 3, the simulation results of the robustness against induced charges of the vertical superjunction MOSFET according to the first embodiment including four guard rings are described. For example, "7.5E+11" on the horizontal axis of FIG. 3 represents " 7.5×10^{11} ". The results described in FIG. 3 indicate that even when surface charges of $\pm 5 \times 10^{11} \text{ cm}^{-2}$ exist, the vertical superjunction MOSFET according to the first embodiment maintains the breakdown voltage equivalent to the breakdown voltage with no charges. By setting the width of p-type semiconductor region **22** to be narrower toward the edge of the edge termination section as described above, a superjunction MOSFET that includes a very reliable and low-cost edge termination section **S** is obtained.

Second Embodiment

[0050] Now a vertical superjunction MOSFET according to a second embodiment of the invention will be described below with reference to FIGS. 4 and 5. FIG. 4 is a top plan view showing a quarter of the vertical superjunction MOSFET according to a second embodiment of the invention. FIG. 5 is a cross sectional view cut along the broken line B-B' in FIG. 4.

[0051] The vertical superjunction MOSFET according to the second embodiment is different from the vertical superjunction MOSFET according to the first embodiment in that the pitch **P2** in alternating-conductivity-type layer **50b** in the edge termination section **S** is smaller than the pitch **P1** in alternating-conductivity-type layer **50a** in the active section **K** in the vertical superjunction MOSFET according to the second embodiment. The vertical superjunction MOSFET according to the second embodiment is different from the vertical superjunction MOSFET according to the first embodiment also in that the widths of the regions in alternat-

ing-conductivity-type layer **50b** do not change gradually but instead change every region group in the vertical superjunction MOSFET according to the second embodiment. In other words, the p-type semiconductor region width becomes narrower than the n-type semiconductor region width in the middle of the edge termination section **S**.

[0052] The vertical superjunction MOSFET according to the second embodiment differs from the vertical superjunction MOSFET according to the first embodiment further in that electrically conductive (metal) field plates **33a**, **33b**, and **33c** are in electrical contact with the surfaces of all the p-type guard rings **32a**, **32b**, and **32c** in the vertical superjunction MOSFET according to the second embodiment.

[0053] If the pitch in alternating conductivity type layer **50b** becomes smaller from the pitch **P1** in alternating conductivity type layer **50a** to the pitch **P2** as described above, the distance between p-type semiconductor regions **22** becomes narrower and the electric field is liable to relax. Therefore, it is easy to obtain a higher breakdown voltage.

[0054] Electrically conductive (metal) field plates **33a**, **33b**, and **33c** in electrical contact with the surfaces of p-type guard rings **32a**, **32b**, and **32c** relax the electric field of p-type guard rings **32a**, **32b**, and **32c** and prevent the depletion layer from expanding. Further, electrically conductive (metal) field plates **33a**, **33b**, and **33c** collect the electric charges caused from the outside. Therefore, electrically conductive (metal) field plates **33a**, **33b**, and **33c** suppress the breakdown voltage variations and improve the robustness against induced charges for the breakdown voltage. Since the p-type semiconductor region **22** width becomes narrower, although stepwise, from the active section **K** side toward the edge of the edge termination section **S**, the vertical superjunction MOSFET according to the second embodiment exhibits the same effects which the vertical superjunction MOSFET according to the first embodiment exhibits.

Third Embodiment

[0055] Now a vertical superjunction MOSFET according to a third embodiment of the invention will be described below with reference to FIG. 6. FIG. 6 is the cross sectional view of a vertical superjunction MOSFET according to a third embodiment of the invention.

[0056] The vertical superjunction MOSFET according to the third embodiment is different from the vertical superjunction MOSFET according to the second embodiment in that the vertical superjunction MOSFET according to the third embodiment includes polysilicon field plates **34a**, **34b**, and **34c**, in stead of metal field plate **33a**, **33b**, and **33c**, in electrical contact with guard rings **32a**, **32b**, and **32c**. For the patterning of polysilicon, a dry etching technique such as reactive ion etching (RIE) is employed. Since the dry etching facilitates improving the dimensional accuracy, the initial breakdown voltage and the robustness against induced charges for breakdown voltage are stabilized effectively.

[0057] According to the first through third embodiments of the invention, an alternating-conductivity-type layer, in which the p-type semiconductor region width becomes narrower from the active section side toward the edge of the edge termination section, is arranged in the edge-termination section that facilitates improving the tradeoff relationship between the on-resistance and the breakdown voltage greatly. Therefore, the superjunction MOSFET according to the invention includes a low-cost edge-termination section that